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Effective on 12/08/2004.
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FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/887,021-Conf. #6645
Filing Date	June 25, 2001
First Named Inventor	Terry R. Lee
Examiner Name	T. U. Vu
Art Unit	2111
Attorney Docket No.	M4065.0407/P407

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
33 - 35 =		x	=

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
10 - 10 =		x	=

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
- 100 =		/50 (round **up** to a whole number) x		=

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY

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TRANSMITTAL OF APPEAL BRIEF

Docket No.
M4065.0407/P407

In re Application of: Terry R. Lee

Application No.	Filing Date	Examiner	Group Art Unit
09/887,021-Conf. #6645	June 25, 2001	T. U. Vu	2111

Invention: SHIELDED ROUTING TOPOLOGY FOR HIGH SPEED MODULES

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: September 29, 2006 .

The fee for filing this Appeal Brief is $ 500.00 .

[X] Large Entity [ ] Small Entity

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The fee for the extension of time is _____ .

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This sheet is submitted in duplicate.

Dated: November 30, 2006

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Docket No.: M4065.0407/P407
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Terry R. Lee

Application No.: 09/887,021 | Confirmation No.: 6645

Filed: June 25, 2001 | Art Unit: 2111

For: SHIELDED ROUTING TOPOLOGY FOR HIGH SPEED MODULES | Examiner: T. U. Vu

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is being filed within one month from the mailing of the Notice of Panel Decision from Pre-Appeal Brief Review, mailed on October 31, 2006, and is in furtherance of the Notice of Appeal filed on September 29, 2006.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is MICRON TECHNOLOGY, INC., the assignee of the application.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 33 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 21 and 34

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-20, 22-33, and 35

4. Claims allowed: None

5. Claims rejected: 1-20, 22-33, and 35

C. Claims On Appeal

The claims on appeal are claims 1-20, 22-33, and 35.

IV. STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the June 29, 2006 Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention relates to a bus routing topology for a bus system in which every pair of signal lines are provided with shielding, thereby effectively limiting signal cross-talk to only one signal pair while minimizing the number of pins required on a connector. By shielding only every pair of signal lines, the number of connector pins is significantly reduced, thus reducing the size and cost of the connector and module on which the connector is provided. (Present Application, Abstract). FIG. 4 from the present application is reproduced below to better explain the claimed subject matter. FIG. 4 has been modified to highlight an aspect of the claimed subject matter discussed below.

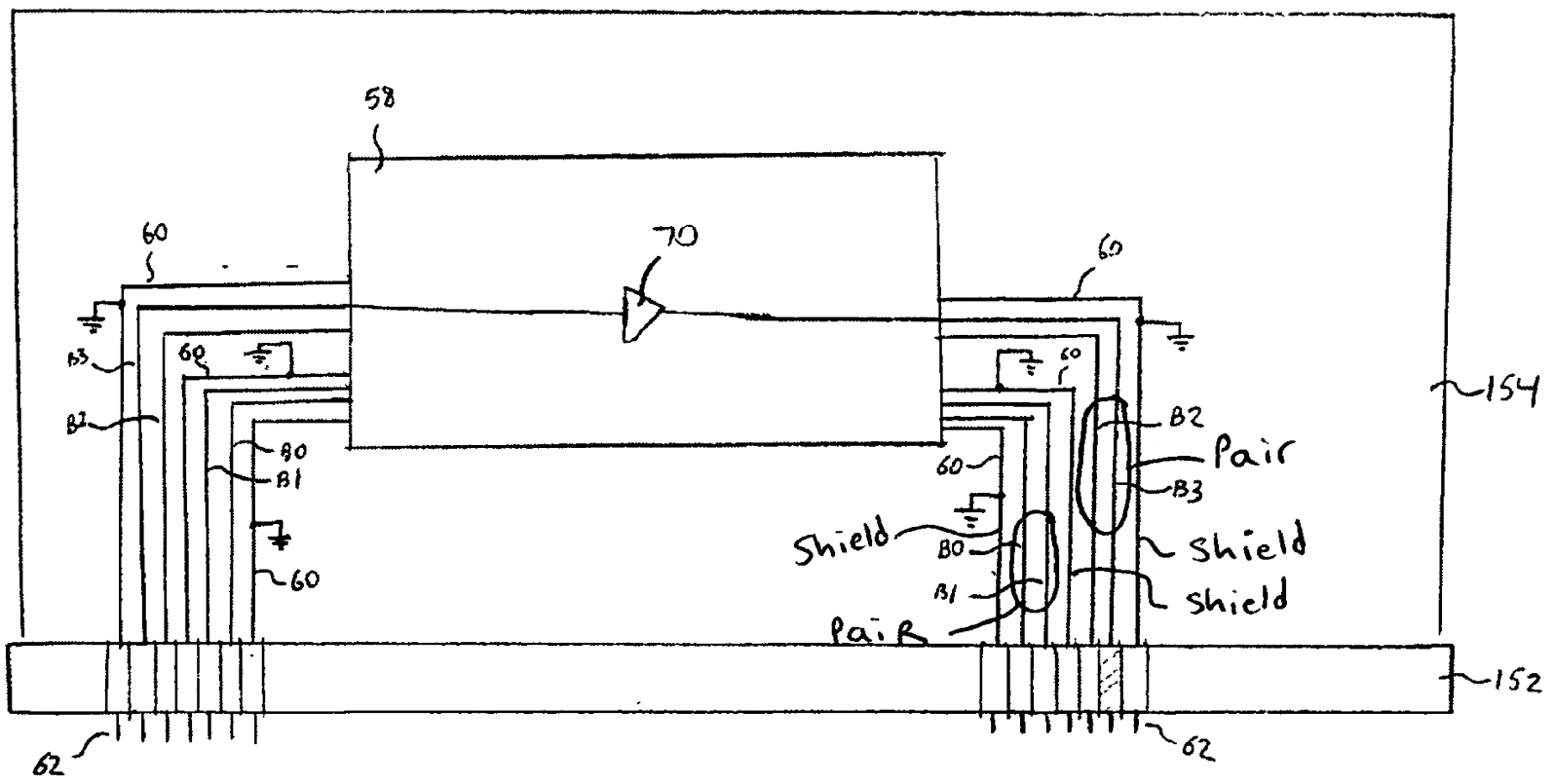

FIG. 4

Claim 1 is drawn to a circuit card 154 that comprises a circuit element 58, supported by the circuit card 154, which has a plurality of inputs and outputs. The circuit card 154 also comprises a plurality of signal lines (B0, B1, B2, and B3) supported by the circuit card 154. Each signal line being electrically connected respectively to one of the plurality of inputs or one of the plurality of outputs. The circuit card 154 also comprises a plurality of shields 60 supported by the circuit card 154, wherein the signal lines are grouped in a plurality of adjacent corresponding pairs, a shield 60 being located respectively on each side of each of the plurality of corresponding pairs of signal lines. (Present Application, paragraph [0024]).

Other embodiments, including a method for constructing a bus system device, and processor systems including the bus system, are recited in additional independent claims. (Present Application, paragraph [0029]). Independent claim 6 recites a "circuit card comprising: a plurality of signal lines supported by the circuit card, each signal line being arranged and configured to be electrically connected at a first end respectively to one of a plurality of connectors of a connector device

mounted on a printed circuit board; a circuit element mounted to the circuit card and having a plurality of inputs and outputs, said signal lines being electrically connected at a second end respectively to one of said plurality of inputs or outputs; and a plurality of shields supported by said circuit card, the shields being arranged and configured on said circuit card to be electrically connected at a first end to respective connectors of said connector device mounted on said printed circuit board, each shield being electrically connected at a second end to a respective one of said plurality of circuit element inputs or outputs." According to claim 6, "said signal lines [are] grouped in a plurality of adjacent corresponding pairs, respective ones of said shields being located on each side of each of said plurality of corresponding pairs of said signal lines." (Present Application, paragraph [0024]).

Independent claim 8 recites a "circuit card comprising: a plurality of signal lines on the circuit card and having a length arranged and configured to connect between a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs; and a shield on the circuit card extending adjacent and the length of each respective signal line pair." The signal lines of claim 8 are "part of a bus system." (Present Application, paragraph [0023]).

Independent claim 11 recites a "memory expansion card comprising: a memory device supported by the expansion card and having a plurality of inputs and outputs; a plurality of signal lines supported by the expansion card, each of said plurality of inputs and outputs of said memory device being coupled to a respective one of said signal lines, said signal lines being grouped in a plurality of adjacent corresponding pairs; and a plurality of shields on the expansion card and electrically connected to said memory device." According to claim 11, a shield is located "respectively between each pair of said plurality of corresponding pairs of said

signal lines; wherein said plurality of signal lines is part of a bus system." (Present Application, paragraph [0024]).

Independent claim 15 recites a "memory expansion card comprising: a memory device supported by said expansion card and having a plurality of inputs and outputs; a plurality of signal lines supported by said expansion card, each signal line connected respectively to one of said inputs or outputs, said plurality of signal lines being grouped respectively in adjacent corresponding pairs; and a plurality of shields supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shields being located to extend along and between each of said plurality of corresponding pairs of said signal lines." According to claim 15, "said plurality of signal lines is part of a bus system." (Present Application, paragraph [0023]).

Independent claim 18 recites a "memory expansion card assembly comprising: a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield, said connectors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors; a plurality of signal lines on said expansion card being connected respectively to each of said first portion of connectors; and a plurality of shields on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors." The "first portion of connectors is part of a bus system." (Present Application, paragraph [0024]).

Independent claim 19 recites a "processing system comprising: a processing unit; a connector device having a plurality of pins and electrically connected to said processing unit and a circuit card coupled to said processing unit through said connector device, said circuit card comprising: a circuit element supported by the circuit card and having a plurality of inputs and outputs; a plurality of signal lines supported by the circuit card, each of said plurality of signal lines being coupled respectively between one of said plurality of inputs and one of said plurality of pins, or one of said plurality of outputs and one of said plurality of pins; and a plurality of shields supported by the circuit card, each shield being connected respectively to said circuit element." The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield being located between respective corresponding pairs of said signal lines." According to claim 19, "said processing system comprises a bus system for passing signals through said processing system and said signal lines are coupled to said bus system." (Present Application, paragraph [0030]).

Independent claim 26 recites a "processing system comprising: a processing unit; and a memory expansion card coupled to said processing unit, said memory expansion card comprising: a memory device supported on said memory expansion card and having a plurality of inputs and outputs; a connector device having a plurality of connectors for electrically coupling said memory expansion card to said processing unit; and a plurality of signal lines and a plurality of shields supported by said memory expansion card, each of a first portion of said plurality of inputs and outputs of said memory device being coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device." The signal lines are "grouped in a plurality of corresponding pairs, a shield being located on each respective side of each of said plurality of corresponding pairs of said signal lines." According to claim 26, "said processing system comprises a bus

system for passing signals through said processing system and wherein said first portion of said plurality of inputs and outputs is coupled to said bus system." (Present Application, paragraph [0030]).

Independent claim 30 recites a "processing system comprising: a processing unit; and a memory expansion card coupled to said processing unit, said memory expansion card comprising: a memory device having a plurality of inputs and a plurality of outputs; a plurality of signal lines supported by said expansion card and connected respectively to said plurality of inputs and outputs, said plurality of signal lines being grouped in a plurality of adjacent corresponding pairs; and a plurality of shields supported by said expansion card and electrically connected to said memory device, a respective one of said plurality of shields being located to extend along each of said plurality of corresponding pairs of said plurality of signal lines." According to claim 30, "said plurality of signal lines is part of a bus system of said processing system." (Present Application, paragraph [0030]).

Independent claim 33 recites a "method for constructing on a circuit card a bus system device comprising the steps of: providing a circuit element on said circuit card, said circuit element having a first plurality of connectors for conducting bus signals; grouping said first plurality of connectors into a plurality of corresponding pairs; and providing a second plurality of connectors on said circuit element, said second plurality of connectors being connected to a respective shield supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors." (Present Application, paragraph [0024]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The first ground of rejection to be reviewed on appeal is the rejection of claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31, and 33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,658,530 ("Robertson") in view of Alleged Admitted Prior Art ("AAPA").

B. The second ground of rejection to be reviewed on appeal is the rejection of dependent claims 3 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Robertson in view of the AAPA and further in view of Chin et al., U.S. Patent No. 6,216,205 ("Chin").

C. The third ground of rejection to be reviewed on appeal is the rejection of dependent claims 4, 10, 13, 17, 23, 28, 32, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Robertson and the AAPA in view of Ortega et al., U.S. Patent No. 6,257,587 ("Ortega").

D. The fourth ground of rejection to be reviewed on appeal is the rejection of dependent claim 25 under 35 U.S.C. § 103(a) as being unpatentable over Robertson in view of the AAPA and further in view of Elabd, U.S. Patent No. 6,526,462 ("Elabd").

VII. ARGUMENT

A. The subject matter of Claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31, and 33 would not have been obvious over Robertson in view of the AAPA.

1. Relevant Claim Limitations

Claim 1 recites a circuit card with "a circuit element supported by the circuit card." The circuit element has "a plurality of inputs and outputs," and "a plurality of signal lines supported by the circuit card." Each signal line is "electrically connected respectively to one of said plurality of inputs or one of said

plurality of outputs." A "plurality of shields [is] supported by the circuit card." The signal lines are "grouped in a plurality of adjacent corresponding pairs." A shield is "located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Claim 6 recites a circuit card with "a plurality of shields supported by said circuit card." The shields are "arranged and configured on said printed circuit board to be electrically connected at a first end to respective connectors of said connector device." Each shield is "electrically connected at a second end to a respective one of said plurality of circuit element inputs or outputs." The signal lines are "grouped in a plurality of adjacent corresponding pairs," and "respective ones of said shields [are] located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Claim 8 recites, in pertinent part, a circuit card having "a shield on the circuit card extending adjacent and the length of each respective signal line pair," which are "on the circuit card."

Claim 11 recites a memory expansion card with a memory device. The memory expansion card includes, *inter alia,* "a plurality of shields on the expansion card and electrically connected to said memory device, a shield being located respectively between each pair of [a] plurality of corresponding pairs of [memory device] signal lines."

Claim 15 recites a memory expansion card that includes "a plurality of shields supported by said expansion card and electrically connected to [a] memory device." Respective shields are "located to extend along and between each of [a] plurality of corresponding pairs of . . . signal lines."

Claim 18 recites a memory expansion card assembly that includes, *inter alia*, "a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield, said connectors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors," "a plurality of signal lines on said expansion card being connected respectively to each of said first portion of connectors," and "a plurality of shields on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors."

Claim 19 recites a processing system that includes, *inter alia*, "a plurality of shields supported by [a] circuit card, each shield being connected respectively to [a] circuit element, [and] signal lines being grouped in a plurality of adjacent corresponding pairs." According to claim 19, a shield is "located between respective corresponding pairs of said signal lines."

Claim 26 recites a processing system that includes a memory expansion card with "a plurality of signal lines and a plurality of shields supported by said memory expansion card." Each of a first portion of said plurality of inputs and outputs of said memory device is "coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device." The signal lines are "grouped in a plurality of corresponding pairs." A shield is "located on each respective side of each of said plurality of corresponding pairs of said signal lines."

Claim 30 recites a processing system that includes a memory expansion card and "a plurality of shields supported by said expansion card and electrically

connected to said memory device." A "respective one of said plurality of shields" is "located to extend along each of said plurality of corresponding pairs of [a] plurality of signal lines."

Claim 33 recites a "method for constructing on a circuit card a bus system device." The method includes steps of "providing a circuit element on said circuit card." The circuit element has "a first plurality of connectors for conducting bus signals" grouped "into a plurality of corresponding pairs." A second plurality of connectors provided on the circuit element is "connected to a respective shield supported on said circuit card." A respective shield extends "along each side of respective pairs of signal lines supported on said circuit card" and "connected to each of said corresponding pairs of said first plurality of connectors."

2. There is no motivation to combine Robertson with the AAPA.

FIG. 1A from Robertson is reproduced below to better explain the disclosure of Robertson. Robertson discloses a memory module 100. The memory module 100 includes printed circuit board (PCB) 101 and a connector 102. The PCB 101 features signal traces 103 that are arranged to be as short as possible. The PCB 101 includes a power layer, an electrical ground layer, and a plurality of signal layers. (Robertson, col. 4, lines 20-21). Robertson uses a large number of ground pins to improve signal integrity by minimizing cross-talk between signal pins. (Robertson, col. 2, lines 49-50). Robertson accomplishes this by teaching a grounding arrangement that involves ground pins 106 that are part of the connector 102. Because Robertson does not show Appellant's claimed shielding, the Final Rejection is forced to combine Robertson with alleged teachings in the AAPA.

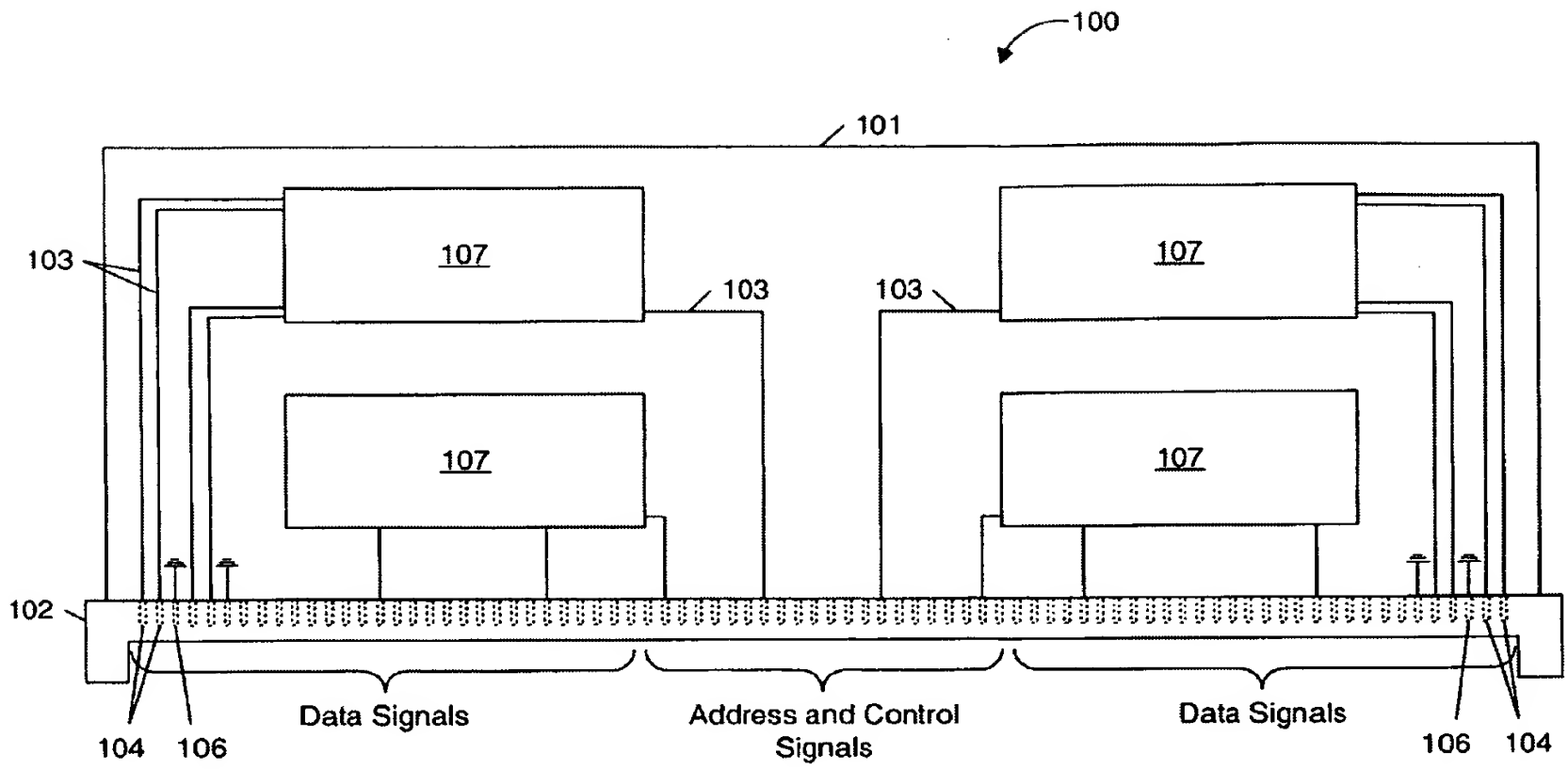

FIG. 1A

The AAPA, however, as shown in Appellant's FIG. 3 (reproduced below), merely teaches using a ground shield 60 for every signal line. The AAPA shields 60 extend the length of a signal line and are supported by the circuit card 54. The AAPA, however, teaches reducing signal cross-talk by providing the shields 60 next to each signal line on the bus. It is clear that the shields taught by the AAPA are designed to reduce cross-talk. If one of ordinary skill in the art follows the teachings of Robertson, one would not be motivated to follow the teachings of the AAPA to add shields that extend the entire length of the signal to the circuit cards, but would instead be motivated by Robertson to eliminate the shields of the AAPA and simply provide ground connector pins, as Robertson teaches, to eliminate cross-talk. Therefore, there is no motivation or suggestion to combine Robertson with the AAPA. The two methods are simply incompatible.

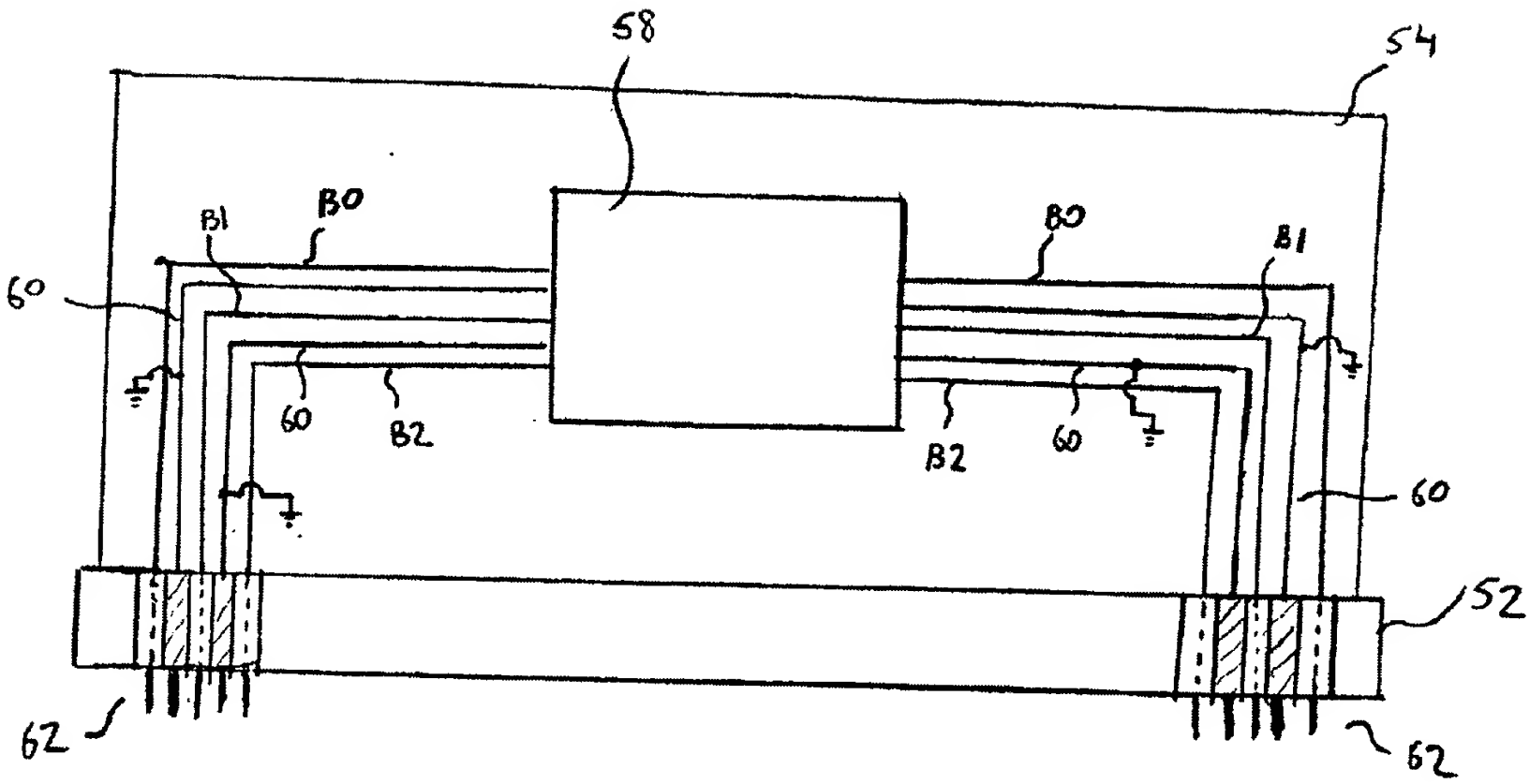

FIG 3
-PRIOR ART-

The June 29, 2006 Final Rejection, however, states that there is motivation to combine the AAPA and Robertson because "one of ordinary skill in the art would recognize the benefit of having the entire length of signal lines shielded to reduce cross-talk along the entire signal lines compared to just reduce cross-talk at the pins." (June 29, 2006 Final Rejection, pages 10-11). Appellant respectfully disagrees and traverses this argument.

For reasons explained above, there is no motivation to combine the cited references to obtain the invention of claims 1, 6, 8, 11, 15, 18, 19, 26, 30, and 33. Motivation or suggestion to combine or modify prior art references "must be clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1334 (Fed. Cir. 2002). Because the "genius of invention is often a combination of known elements which in hindsight seems preordained," the Federal Circuit requires a "rigorous application of the requirement

for a showing of the teaching or motivation to combine prior art references." *McGinley*, 262, F.3d at 1351. Yet there is no teaching or suggestion within any of the references that provide a motivation to combine them.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Thus, a showing of an obvious combination requires more than just an amalgam of references, each of which provides one feature of the claimed invention.

The Final Rejection has done no more than cite a pair of references, each of which allegedly provides only part of the claimed invention, and allege that their combination renders the invention obvious. However, without the benefit of hindsight, there would have been no motivation to combine these references and the Final Rejection has failed to provide proof of any such motivation. This is one more reason why claims 1, 6, 8, 11, 15, 18, 19, 26, 30, and 33 are allowable over the cited combination.

Accordingly, the rejection of claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31, and 33 should be reversed.

3. Robertson teaches away from its combination with the AAPA.

Appellant respectfully submits that Robertson is not properly combinable with the AAPA because Robertson teaches away from the cited combination. The Federal Circuit has held that it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). This is the case we have here.

Robertson teaches reducing or eliminating cross-talk by adding ground connector pins 106 to a connector 102 between groups of signal lines. (Robertson, col. 4, lines 65-66). Therefore, Robertson teaches away from adding shields on a PCB

card as in the AAPA. Robertson's signal traces are not shielded at all on the card, and Robertson does not suggest that they should be, or need be, shielded on the card to eliminate cross-talk.

Furthermore, Robertson teaches eliminating the shields of the AAPA from the card because the properties of the ground pins 106 and the shields 60 of the AAPA vary. For instance, the ground pin 106 is connected to an electrical ground layer (Robertson, col. 4, line 21) of PCB 101. Also, the pin 106 is located as part of the *connector* 102, and not supported by the circuit card 54 as in the AAPA. Further, the ground pin 106 provides a "low resistance path for return currents from the memory module." (Robertson, col. 3, lines 60-64). The AAPA, on the other hand, teaches that the shields on the card provide a coupling path from the signal lines to ground. (Present Application, paragraph [0009]). Appellant submits that because the properties of Robertson and the AAPA vary and because Robertson specifically does away with shielding supported on the card, Robertson teaches away from using the AAPA shielding. Accordingly, Robertson is not properly combinable with the AAPA.

Accordingly, this is another reason why the rejection of claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31, and 33 should be reversed.

B. The subject matter of Claims 3 and 22 would not have been obvious over Robertson in view of the AAPA and further in view of Chin.

1. Claim 3 depends from claim 1 and claim 22 depends from claim 19.

Claim 3 depends from claim 1 and is therefore allowable for at least the same reasons as discussed above with regard to claim 1. Claim 22 depends from claim 19 and is therefore allowable for at least the same reasons as discussed above with regard to claim 19. As such, the rejection should be reversed.

2. Robertson in view of the AAPA and Chin does not teach all the recited elements of claims 3 and 22.

In addition, the Final Rejection has failed to make a prima facie case for obviousness regarding claims 3 and 22 because the combination of Robertson in view of the AAPA and Chin does not teach or suggest a circuit card with "a plurality of shields supported by the circuit card" where a plurality of signal lines supported by the circuit card" are "grouped in plurality of adjacent corresponding pairs" and a shield is "located respectively on each side of each of said plurality of corresponding pairs of said signal lines," as recited in claims 1 and 19. Chin has been cited as providing a driver to drive signals between inputs and outputs of the circuit element. (June 29, 2006 Final Rejection, page 6). As such, Chin does not remedy the deficiencies of the Robertson and AAPA combination.

Therefore, the cited combination does not teach or suggest a circuit card with "a plurality of shields supported by the circuit card" where a plurality of signal lines supported by the circuit card" are "grouped in plurality of adjacent corresponding pairs" and a shield is "located respectively on each side of each of said plurality of corresponding pairs of said signal lines," as recited in claims 1 and 19.

Accordingly, this is another reason why the rejection of claims 3 and 22 should be reversed.

C. The subject matter of Claims 4, 10, 13, 17, 23, 28, 32, and 35 would not have been obvious over Robertson in view of the AAPA and further in view of Ortega.

1. Claims 4, 10, 13, 17, 23, 28, 32, and 35 depend from claims 1, 8, 11, 15, 19, 26, 30, and 33, respectively.

Claims 4, 10, 13, 17, 23, 28, 32, and 35 depend from claims 1, 8, 11, 15, 19, 26, 30, and 33, respectively and are therefore allowable for at least the same reasons

as discussed above with regard to claims 1, 8, 11, 15, 19, 26, 30, and 33. As such, the rejection should be reversed.

2. Robertson in view of the AAPA and Ortega does not teach all the recited elements of claims 4, 10, 13, 17, 23, 28, 32, and 35.

In addition, the Final Rejection has failed to make a prima facie case for obviousness regarding claims 4, 10, 13, 17, 23, 28, 32, and 35 because the combination of Robertson in view of the AAPA and Ortega does not teach or suggest a circuit card with shields supported by the circuit card where signal lines supported by the circuit card are grouped in corresponding pairs and a shield is located respectively on each side of each of the corresponding pairs of the signal lines. Ortega has been cited as implementing differential signals to suppress signal noise or cross-talk. (June 29, 2006 Final Rejection, page 7). As such, Ortega does not remedy the deficiencies of the Robertson and AAPA combination. Therefore, the cited combination does not teach or suggest at least this limitation.

Accordingly, this is another reason why the rejection of claims 4, 10, 13, 17, 23, 28, 32, and 35 should be reversed.

D. The subject matter of Claim 25 would not have been obvious over Robertson in view of the AAPA and further in view of Elabd.

1. Claim 25 depends from claim 19.

Claim 25 depends from claim 19 and is therefore allowable for at least the same reasons as discussed above with regard to claim 19. As such, the rejection should be reversed.

2. Robertson in view of the AAPA and Elabd does not teach all the recited elements of claim 25.

In addition, the Final Rejection has failed to make a prima facie case for obviousness regarding claim 25 because the combination of Robertson in view of the AAPA and Elabd does not teach or suggest a circuit card with "a plurality of shields

supported by the circuit card" where a plurality of signal lines supported by the circuit card" are "grouped in plurality of adjacent corresponding pairs" and a shield is "located respectively on each side of each of said plurality of corresponding pairs of said signal lines," as recited in claim 19. Elabd has been cited as implementing a processor, memory, and control unit on the same chip. (June 29, 2006 Final Rejection, page 10). As such, Elabd does not remedy the deficiencies of the Robertson and AAPA combination.

Therefore, the cited combination does not teach or suggest a circuit card with "a plurality of shields supported by the circuit card" where a plurality of signal lines supported by the circuit card" are "grouped in plurality of adjacent corresponding pairs" and a shield is "located respectively on each side of each of said plurality of corresponding pairs of said signal lines," as recited in claim 19.

Accordingly, this is another reason why the rejection of claim 25 should be reversed.

CONCLUSION

For each of the foregoing reasons, Appellant respectfully submits that the claimed subject matter is not unpatentable over the cited combination. Appellant respectfully requests the reversal of the final grounds of rejection.

Dated: November 30, 2006

Respectfully submitted,

By _____

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VIII. CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 09/887,021

1. (Previously presented) A circuit card comprising:

a circuit element supported by the circuit card, the circuit element having a plurality of inputs and outputs;

a plurality of signal lines supported by the circuit card, each signal line being electrically connected respectively to one of said plurality of inputs or one of said plurality of outputs; and

a plurality of shields supported by the circuit card;

wherein said signal lines are grouped in a plurality of adjacent corresponding pairs, a shield being located respectively on each side of each of said plurality of corresponding pairs of said signal lines.

2. (Previously presented) The circuit card according to claim 1, wherein each said shield is a ground shield.

3. (Previously presented) The circuit card according to claim 1, wherein said circuit element further comprises:

a driver to drive signals between said inputs and said outputs of said circuit element.

4. (Previously presented) The circuit card according to claim 1, wherein said signal lines are arranged and configured such that signals in each of said corresponding pairs of signal lines are differential signals.

5. (Previously presented) The circuit card according to claim 1, wherein said circuit element is a memory device.

6. (Previously presented) A circuit card comprising:

a plurality of signal lines supported by the circuit card, each signal line being arranged and configured to be electrically connected at a first end respectively to one of a plurality of connectors of a connector device mounted on a printed circuit board;

a circuit element mounted to the circuit card and having a plurality of inputs and outputs, said signal lines being electrically connected at a second end respectively to one of said plurality of inputs or outputs; and

a plurality of shields supported by said circuit card, the shields being arranged and configured on said circuit card to be electrically connected at a first end to respective connectors of said connector device mounted on said printed circuit board, each shield being electrically connected at a second end to a respective one of said plurality of circuit element inputs or outputs;

said signal lines being grouped in a plurality of adjacent corresponding pairs, respective ones of said shields being located on each side of each of said plurality of corresponding pairs of said signal lines.

7. (Previously presented) The circuit card according to claim 6, wherein said shields are ground shields.

8. (Previously presented) A circuit card comprising:

a plurality of signal lines on the circuit card and having a length arranged and configured to connect between a connector device and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs; and

a shield on the circuit card extending adjacent and the length of each respective signal line pair;

wherein said signal lines are part of a bus system.

9. (Previously presented) The circuit card according to claim 8, wherein said shields are ground shields.

10. (Previously presented) The circuit card according to claim 8, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

11. (Previously presented) A memory expansion card comprising:

a memory device supported by the expansion card and having a plurality of inputs and outputs;

a plurality of signal lines supported by the expansion card, each of said plurality of inputs and outputs of said memory device being coupled to a respective one of said signal lines, said signal lines being grouped in a plurality of adjacent corresponding pairs; and

a plurality of shields on the expansion card and electrically connected to said memory device, a shield being located respectively between each pair of said plurality of corresponding pairs of said signal lines;

wherein said plurality of signal lines is part of a bus system.

12. (Previously presented) The memory expansion card according to claim 11, wherein each said shield is a ground shield.

13. (Previously presented) The memory expansion card according to claim 11, wherein signals to be transmitted in each of said corresponding pairs of adjacent signal lines are differential signals.

14. (Previously presented) The memory expansion card according to claim 11, wherein said expansion card is adapted for connection to a motherboard.

15. (Previously presented) A memory expansion card comprising:

a memory device supported by said expansion card and having a plurality of inputs and outputs;

a plurality of signal lines supported by said expansion card, each signal line connected respectively to one of said inputs or outputs, said plurality of signal lines being grouped respectively in adjacent corresponding pairs; and

a plurality of shields supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shields being located to extend along and between each of said plurality of corresponding pairs of said signal lines;

wherein said plurality of signal lines is part of a bus system.

16. (Previously presented) The memory expansion card according to claim 15, wherein each said shield is a ground shield.

17. (Previously presented) The memory expansion card according to claim 15, wherein said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

18. (Previously presented) A memory expansion card assembly comprising:

a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield, said connectors in said first portion being grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors;

a plurality of signal lines on said expansion card being connected respectively to each of said first portion of connectors; and

a plurality of shields on said expansion card being connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors,

wherein said first portion of connectors is part of a bus system.

19. (Previously presented) A processing system comprising:

a processing unit;

a connector device having a plurality of pins and electrically connected to said processing unit and

a circuit card coupled to said processing unit through said connector device, said circuit card comprising:

a circuit element supported by the circuit card and having a plurality of inputs and outputs;

a plurality of signal lines supported by the circuit card, each of said plurality of signal lines being coupled respectively between one of said plurality of inputs and one of said plurality of pins, or one of said plurality of outputs and one of said plurality of pins; and

a plurality of shields supported by the circuit card, each shield being connected respectively to said circuit element, said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield being located between respective corresponding pairs of said signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and said signal lines are coupled to said bus system.

20. (Previously presented) The processing system according to claim 19, wherein each said shield is a ground shield.

Claim 21. (Canceled)

22. (Previously presented) The processing system according to claim 19, wherein said circuit element further comprises:

a driver to drive signals between said inputs and said outputs of said circuit element.

23. (Previously presented) The processing system according to claim 19, wherein said circuit element has inputs and outputs for differential signals and said signal lines are arranged and configured such that signals transmitted in each of said corresponding pairs are differential signals.

24. (Previously presented) The processing system according to claim 19, wherein said circuit element is a memory device.

25. (Previously presented) The processing system according to claim 19, wherein said processing unit and said circuit element are on a same chip.

26. (Previously presented) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device supported on said memory expansion card and having a plurality of inputs and outputs;

a connector device having a plurality of connectors for electrically coupling said memory expansion card to said processing unit; and

a plurality of signal lines and a plurality of shields supported by said memory expansion card, each of a first portion of said plurality of inputs and outputs of said memory device being coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device, said signal lines being grouped in a plurality of corresponding pairs, a shield being located on each respective side of each of said plurality of corresponding pairs of said signal lines;

wherein said processing system comprises a bus system for passing signals through said processing system and wherein said first portion of said plurality of inputs and outputs is coupled to said bus system.

27. (Previously presented) The processing system according to claim 26, wherein said shields are ground shields.

28. (Previously presented) The processing system according to claim 26, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

29. (Previously presented) The processing system according to claim 26, further comprising:

a motherboard equipped with a connector adapted for connection of said memory expansion card to said motherboard, the connector comprising connecting pins corresponding respectively to said signal lines and said shields.

30. (Previously presented) A processing system comprising:

a processing unit; and

a memory expansion card coupled to said processing unit, said memory expansion card comprising:

a memory device having a plurality of inputs and a plurality of outputs;

a plurality of signal lines supported by said expansion card and connected respectively to said plurality of inputs and outputs, said plurality of signal lines being grouped in a plurality of adjacent corresponding pairs; and

a plurality of shields supported by said expansion card and electrically connected to said memory device, a respective one of said plurality of shields being located to extend along each of said plurality of corresponding pairs of said plurality of signal lines;

wherein said plurality of signal lines is part of a bus system of said processing system.

31. (Previously presented) The processing system according to claim 30, wherein said shields are ground shields.

32. (Previously presented) The processing system according to claim 30, wherein said signal lines are arranged such that signals in each of said corresponding pairs are differential signals.

33. (Previously presented) A method for constructing on a circuit card a bus system device comprising the steps of:

providing a circuit element on said circuit card, said circuit element having a first plurality of connectors for conducting bus signals;

grouping said first plurality of connectors into a plurality of corresponding pairs; and

providing a second plurality of connectors on said circuit element, said second plurality of connectors being connected to a respective shield supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors.

Claim 34. (Canceled)

35. (Previously presented) The method according to claim 33, further comprising adapting said first plurality of connectors in each corresponding pair to conduct differential signals.

IX. EVIDENCE APPENDIX

Evidence Involved in the Appeal of Application Serial No. 09/887,021

No evidence is being submitted.

X. RELATED PROCEEDINGS APPENDIX

Related Proceedings Involved in the Appeal of Application Serial No. 09/887,021

No related proceedings are referenced and therefore, no copies of decisions in related proceedings are provided.